AN13862

NXP PMIC solution for TI TDA4VM processor

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Document information

Information	Content
Keywords	Power solution, BYLink,TDA4VM, FS86, PF82, PF52, PF5020
Abstract	This application note presents how to use NXP power management integrated circuit (PMIC) FS86 , PF82, PF52, PF5020 to power the TI TDA4VM processor system.

Revision history

Rev	Date	Description
v.1.0	20230317	Initial version

1 Scope of the document

This application note shows the power solution using NXP power management integrated circuit (PMIC) FS86, PF82, PF52, PF5020 to power TI TDA4VM devices. Users learn how to use NXP PMICs to accomplish the power solution design including power rails configuration and functional safety features. This application note also provides a general description of the functional safety interconnection between NXP PMICs and TDA4VM.

2 TDA4VM and NXP PMIC overview

The TDA4VM is a high-performance smart-processing platform targeted at ADAS and Autonomous Vehicle (AV) applications. Given the high number of power rails required, TDA4VM systems present challenging power management demands. These conditions are further complicated by the need to meet the system functional safety requirements. NXP's flexible Power Management ICs (PMIC) offer a total power solution that fully meets TDA4VM power and safety requirements in a way that simplifies design and development.

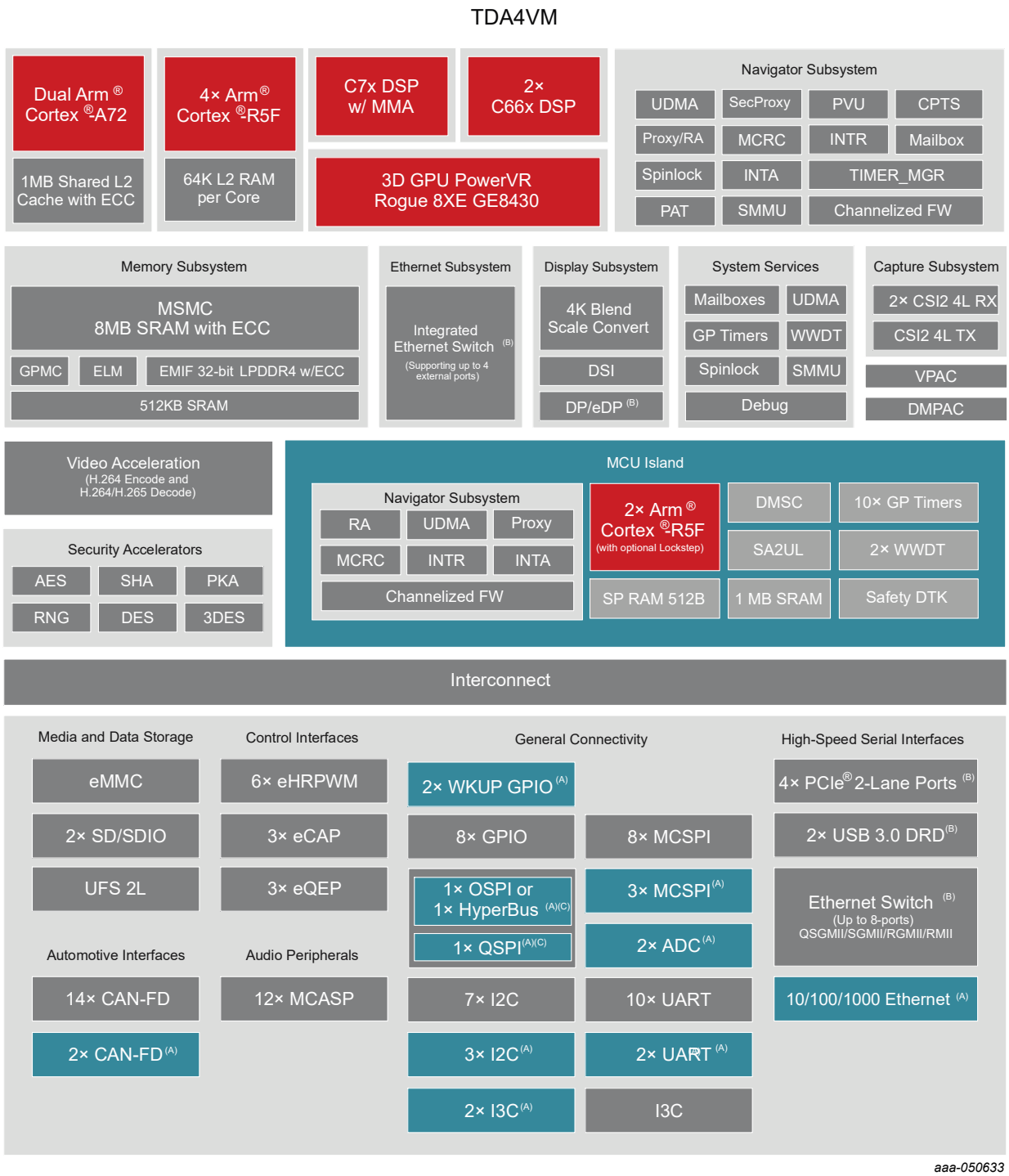

Figure 1. TDA4 block diagram

BYLink system power platform facilitates the design of safe power management systems thanks to a portfolio of configurable and linkable devices. It simplifies complex power supply subsystems into a single smart solution. This allows system level safety integration. BYLink is a simple and effective way to enable complex applications such as ADAS and zone controllers. BYLink platform includes High-voltage PMICs and Low-voltage PMICs. PMICs that can be directly connected to Vbat are High-voltage PMICs or System Basic Chips (SBCs). PMICs that can be connected to maximum 5.5V Vin are Low-voltage PMICs.

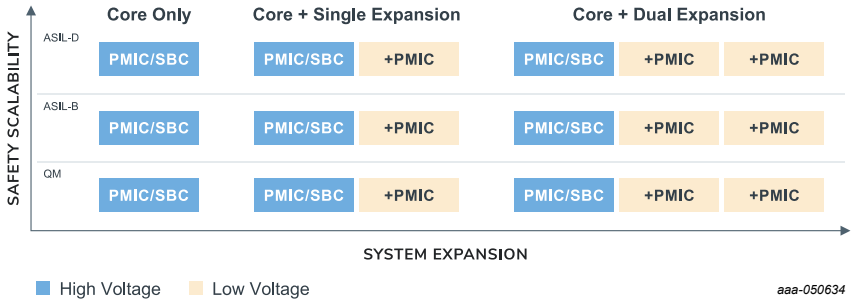

Figure 2. BYLink system power platform

NXP provides a complete portfolio of safety PMICs with embedded system features. FS86, FS85, FS56, and VR5510 can be selected as options of the High-Voltage PMIC. PF PMICs such as PF8x00, PF5200, PF502x Low-Voltage PMICs have similar design structure and are defined to work together in system by logic connection and power companion.

3 TDA4VM power solution introduction

To implement the NXP power solution for TDA4VM, the high-voltage PMIC FS86 working with low-voltage PMICs PF82, PF52, and PF5020 solution is suitable for TDA4VM total system in automotive ADAS or Autonomous driving application.

Figure 3 shows the block diagram of NXP power solution for TDA4VM system. The FS86 integrates a battery connected HV BUCK controller with external FETs and the current capability can achieve 15 A. This HV BUCK can be used as the power supply input of PF PMICs, and FS86 also supplies power to the TDA4VM safety MCU. PF PMICs supply power to the main power domain of the processor to achieve the isolation between the MCU and main power domain.

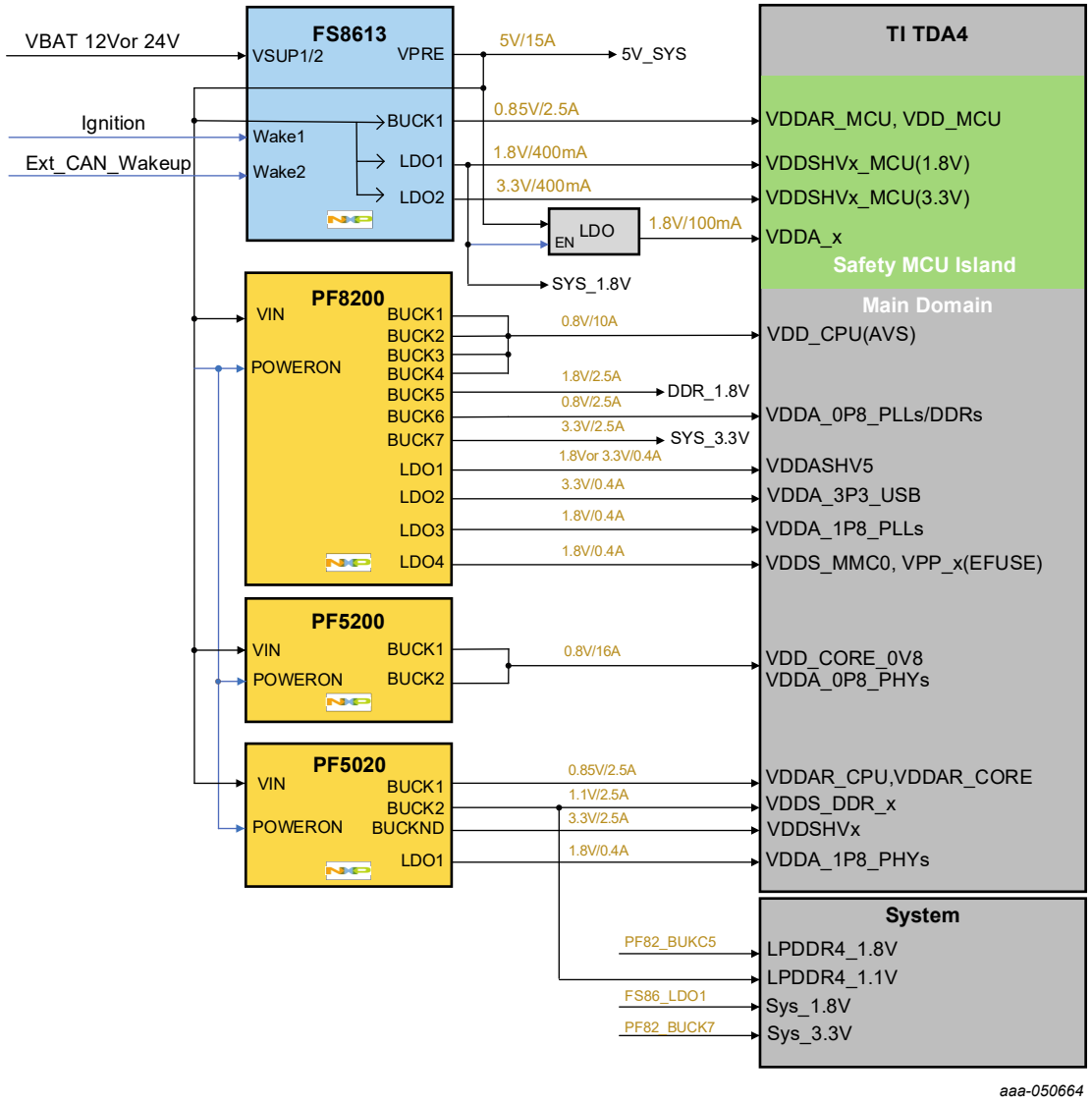

Figure 3. NXP power solution for TI TDA4

4 Power up and power down sequence

Table 1 shows the design parameters of NXP PMICs for TDA4VM solution including detailed PMIC power tree configurations, power up sequences and current capability of each regulator.

Table 1. The design parameters of FS86+PF82+PF52+PF5020 for TDA4VM solution

Device	PMIC Regulator	Voltage(V)	Max load(A)	TDA4 System Power rails	Timer Stamp
FS8600	VPRE	5	15	PF PMIC input	PRE
	SW1	0.85	2.5	VDDAR_MCU VDD_MCU	T3
	LDO1	1.8	0.4	VDDSHx_MCU(1.8V) System_1.8V	T1

Table 1. The design parameters of FS86+PF82+PF52+PF5020 for TDA4VM solution*...continued*

Device	PMIC Regulator	Voltage(V)	Max load(A)	TDA4 System Power rails	Timer Stamp
	LDO2	3.3	0.4	VDDSHx_MCU(3.3V)	T0
External	LDO	1.8	0.1	VDDA_x	T1
PF8200	SW1-4	0.8	10	VDD_CPU(AVS)	T2
	SW5	1.8	2.5	LPDDR4_1.8V	T1
	SW6	0.8	2.5	VDDA_0P8_PLLs/DLLs	T2
	SW7	3.3	2.5	System_3.3V	T0
	LDO1	1.8/3.3	0.4	VDDSHV5	T0
	LDO2	3.3	0.4	VDDA_3P3_USB	T0
	LDO3	1.8	0.4	VDDA_1V8_PLLs	T1
	LDO4	1.8	0.4	VDDS_MMC0 VPP_x(EFUSE)	T1
PF5200	SW1-2	0.8	16	VDD_CORE VDDA_0P8_PHYs	T2
PF5020	SW1	0.85	2.5	VDDAR_CPU VDDAR_CORE	T3
	SW2	1.1	2.5	VDDS_DDR_x LPDDR4_1.1V	T3
	SWND1	3.3	2.5	VDDSHVx	T0
	LDO1	1.8	0.4	VDDA_1P8_PHYs	T1

This section also describes power supply sequencing required to ensure proper device operation. Figure 4 shows the main power up sequence when using NXP PMICs to power a TDA4VM system with isolate MCU and Main voltage domains.

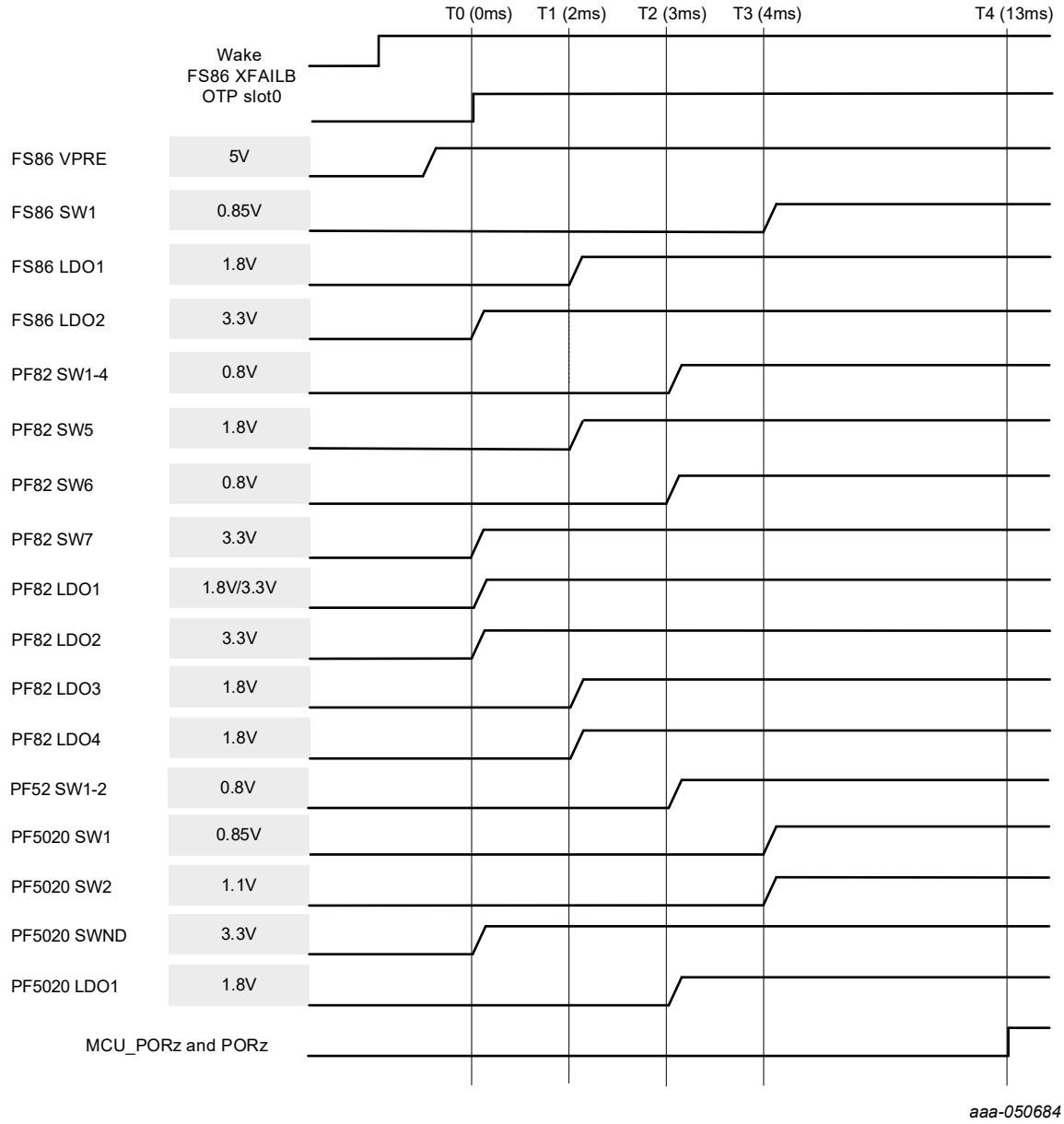

Figure 4. TDA4VM primary power-up sequence, isolate MCU and main domains

NXP PMICs feature a built-in one-time programmable (OTP) memory that stores key startup configurations. Users define the OTP configuration based on their specific application requirements. The default sequence slot for PMICs are programmed via the OTP configuration registers. The sequence slot includes time base and time slot to realize flexible power up\power down sequence configuration.

NXP PMICs feature a dedicated functional block for synchronizing power up sequences from multiple PMICs. XFAILB is a bidirectional pin with an open drain output used to synchronize the power up and power down sequences of multiple PMICs. XFAILB of FS86 should be connected directly to the XFAILB pin of the PF PMICs.

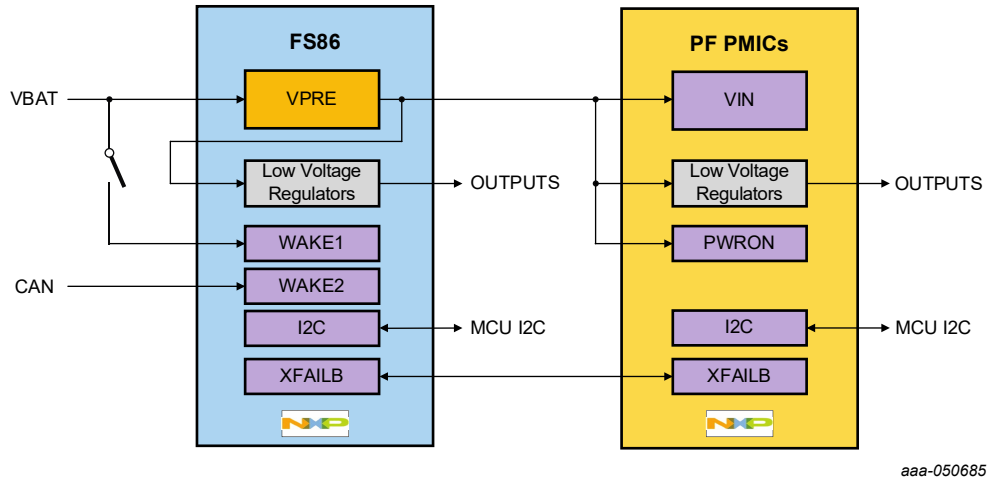

Figure 5. XFAILB connection between FS86 and Low Voltage PMICs

Wake1 of FS86 can be connected with ignition signal and wake2 can be connected with CAN PHY wake up signal. When FS86 is awakened, VPRE BUCK powers up first. As VIN and PWRON of PF PMICs are connected with FS86 VPRE output, the PF devices start up when PWRON is pulled high. PF PMIC regulators and FS86 LV regulators start up following the power up sequence as defined in OTP. FS86 RSTB pin connected with TDV4VM processor MCU_POR and PORz pins are released at the end of the power sequence if all the power rails turn on with no fault. RSTB release delay can be added to accommodate the processor requirement asking for voltage supply stabilization before RSTB is released. The default power down sequence is the power up reverse order, and a specific power down sequence can also be performed through the I2C command.

5 Functional safety

Functional safety is normally required for ADAS or autonomous driving applications. The FS86 is an ASIL-D-ready SBC, and PF52, PF82 and PF5020 are ASIL-B-ready devices. The NXP PMICs listed here are developed in compliance with the IOS26262 standard, and are appropriate for this architecture.

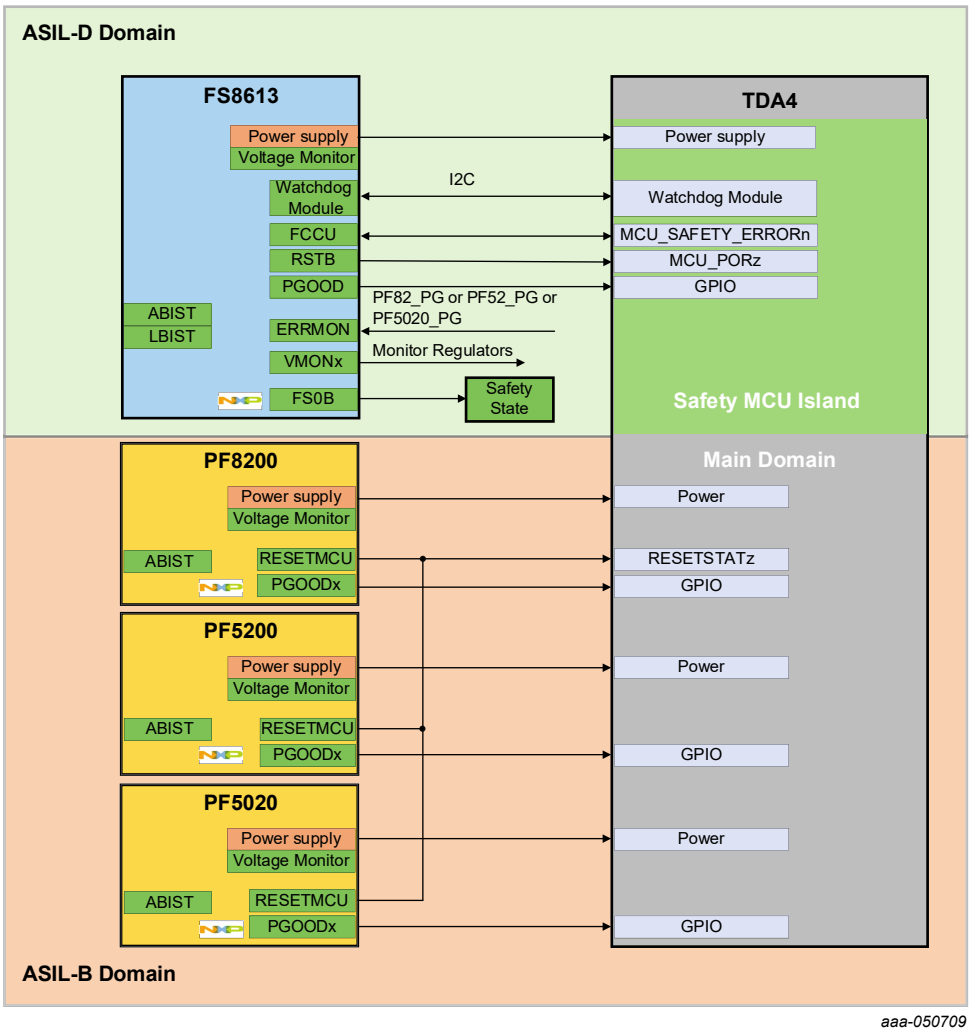

Figure 6. Functional signal connection between PMIC and TDA4VM

Figure 6 shows the recommended functional signal connections between PMIC and TDA4VM processor. The FS86 family and PF series devices implement embedded safety mechanisms that include the functional safety features as follows:

- **Independent voltage monitoring and fault detection**: PMICs feature independent fault monitoring per regulator. Three types of faults (undervoltage (UV), overvoltage (OV), and current limit (ILIM)) are monitored by the PMIC fault monitor block. The PMIC can indicate the output state per regulator through PGOOD.
- **I2C CRC and write protection**: I2C secure write protection protects the secure registers against faulty operation using a dedicated safety mechanism.
- **Analog built-in self-test (ABIST)**: When power to the system is turned on, the PMICs automatically test all output voltage monitors prior to the power up sequence. ABIST checks the state of the voltage monitoring block (OV/UV) per regulator, whether it's normal or not. If a failure on the OV/UV monitor is detected during ABIST, the PMIC asserts the corresponding ABIST flags.
- **VIN OVLO function**: All NXP PMICs feature a Voltage In, Over Voltage Lockout (VIN_OVLO) circuit to monitor the main input supply of the PMIC. The PMIC monitors its input voltage, and can initiate a power down sequence when a VIN_OVLO is detected in the system.

- **Functional safety output**: When a critical fault is detected by the PMIC, such as an incorrect regulator output or watchdog (WD) failure, the Fail-Safe Output 0 (FS0B) pin from FS86 is used to transition the system into a safe state.
- **Logic build-in self-test (LBIST, FS86 only)**: LBIST verifies the correct functionality of the safety logic monitoring. FS86 performs LBIST after power on or upon wakeup from Standby mode.
- **External voltage monitor (FS86 only)**: The FS86 can monitor up to ten voltages, including FS86 supply rails or system PF device regulators. Depending on the safety requirements, voltage monitoring (VMON) can be used to monitor PF device(s), to reach the ASIL-D safety level for the system.
- **MCU failure monitoring (FS86 only)**: The FS86 features two input pins (FCCU1/2) in charge of monitoring hardware failures of the safety MCU. Fault Collection and Control Unit (FCCU) pins can be connected to the Fault output I/O of MCU. When the FS86 detects a hardware failure from MCU through FCCU, the FS86 FS0B\RSTB pin can be asserted.
- **External IC monitoring (FS86 only)**: The FS86 features the ERRMON input pin, in charge of monitoring an external safety IC on the application.
- **Challenger watchdog monitoring (FS86 only)**: The challenger watchdog function is based on a question/answer strategy to monitor the safety MCU.

6 Optional power solution for TDA4VM

To use TI PMICs as the LV PMICs to supply the power to TDA4VM system, refer to the below power solution in Figure 7. FS86 VPRE can output 3.3 V/15 A as TI PMICs input, and FS86 BUCK1 and LDOs can be used to supply power to peripherals. The extended voltage monitoring capability of the FS86 (up to 10 VMONx) can be used to monitor and diagnose regulators in the system which can save the processor resources for monitoring these power rails. Figure 7 power solution has already been used in customer applications.

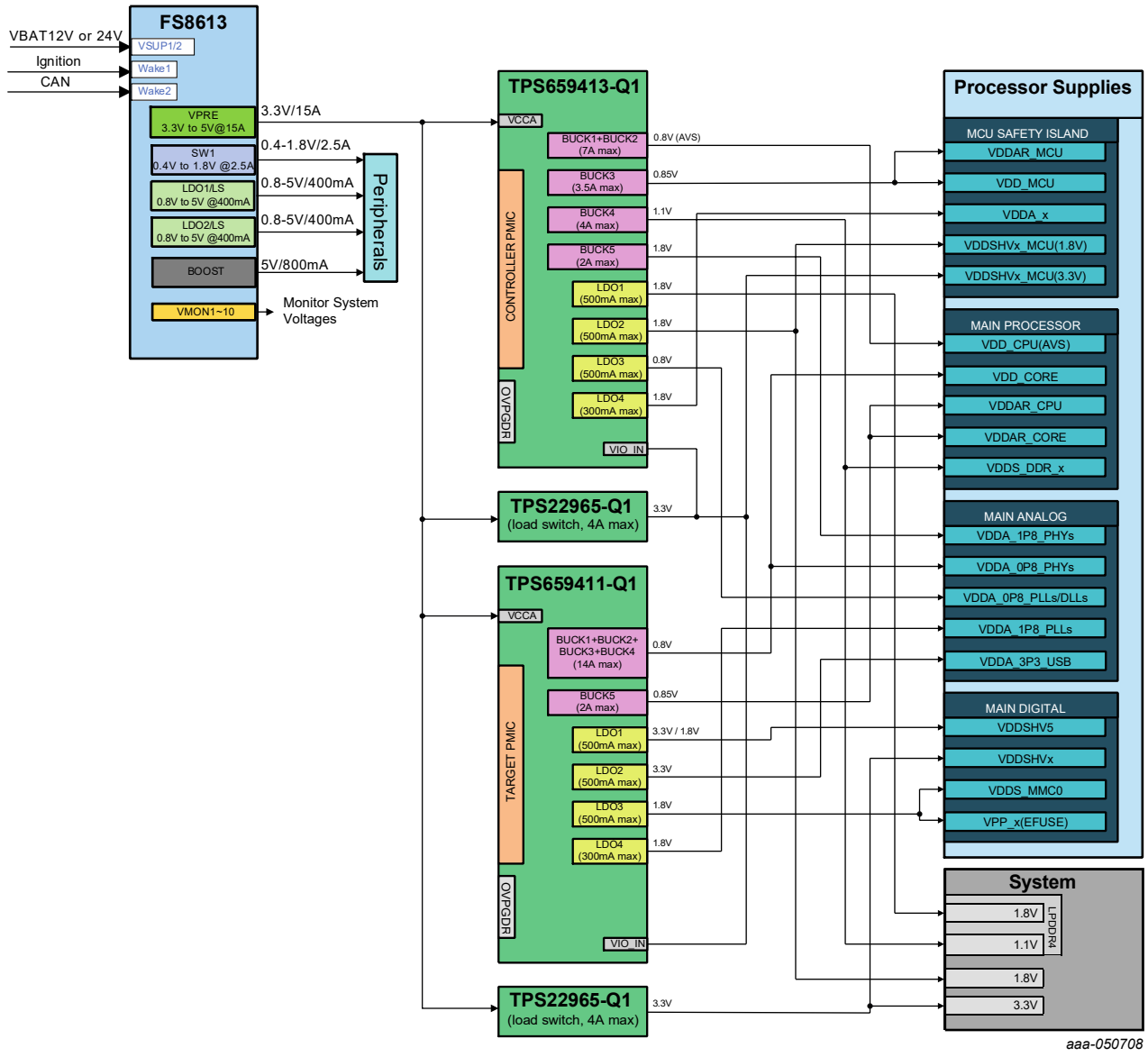

Figure 7. FS86 and TI PMICs supply power to TDA4VM system

7 References

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2. FS82 product summary page: PMIC for High-Performance Applications | NXP Semiconductors
3. PF52 product summary page: PF5200 | Dual-Channel PMIC for Automotive Application | NXP Semiconductors
4. PF5020 product summary page: PF5020 | Multi-Channel (5) PMIC for Automotive | NXP Semiconductors
5. BYLink System Power Platform: https://www.nxp.com/BYLink

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