AN13433

NXP PMIC solution for XILINX UltraScale+ MPSoC ZU11_ZU15 Processor

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Document information

Information	Content
Keywords	Power solution, PMIC, FS86, PF71, PF5023, PF52, Functional safety, Autonomous driving, Xilinx Zynq UltraScale+ MPSoC, ZU11, ZU15
Abstract	This AN presents a cost optimized PMIC solution for a Xilinx Zynq UltraScale + MPSoC ZU11 / ZU15 based system, targeted primarily for autonomous driving applications. It introduces PMIC configuration details and functional features.

Revision history

Rev	Date	Description
v.1	20211108	Initial version

1 Introduction

This application note (AN) shows how to supply a XILINX Zynq UltraScale+ MPSoC series (ZU11/ZU15) processor based system using NXP safety Power Management ICs (PMICs). The application note presents one cost optimized system power solution with four NXP PMICs, including power tree, power up sequence, PMIC / microcontroller unit (MCU) interaction, and functional safety information. The AN also provides the complete PMIC schematic, with the associated BOM.

The Xilinx Zynq UltraScale+ MPSoC ZU11 / ZU15 is a high performance smart processing platform for deep learning, targeted for vehicle autonomous driving applications. Designing a power solution for a processor of this complexity is a challenge, considering the processor's multiple power rails and functional safety capability. This challenge can be addressed using NXP's portfolio of configurable and linkable devices (see BYLink). This NXP multiple PMIC solution can facilitate customer designs by simplifying power solution design and reducing development time. Multiple NXP PMICs can be combined to act as "one chip" to power and secure a ZU11 / ZU15 system.

2 Power solution

One safety MCU is usually needed in a ZU11 / ZU15 based autonomous driving application. The safety MCU directs decision and control functions. This section presents one typical PMIC solution for this type of system. NXP PMICs integrate flexible OTP (One Time Programming), using the BYLink strategy. OTP allows customized configuration of PMIC functions and parameters to meet specific application requirements, which helps customers optimize their designs.

2.1 System power block diagram

This PMIC solution uses FS86, PF52, PF71 and PF5023 series PMICs. Table 1 illustrates the power tree. The FS86 integrates a battery connected pre-regulator that generates intermediate voltages used at the power supply inputs of PF series PMICs. The FS86 also supplies power to the safety MCU. PF52, PF71 and PF 5023 are low input voltage PMICs that offer power to the ZU11 / ZU15.

NXP PMICs have built in OTP memory that stores key startup configurations. Each PMIC also features a dedicated functional block used to synchronize the power up sequence of multiple PMICs. This allows multiple NXP PMICs to work like "one chipset" in the system. Because of this, there is no need for an external controller to configure system default voltage and the power up sequence. This saves design effort and reduces the system's complexity.

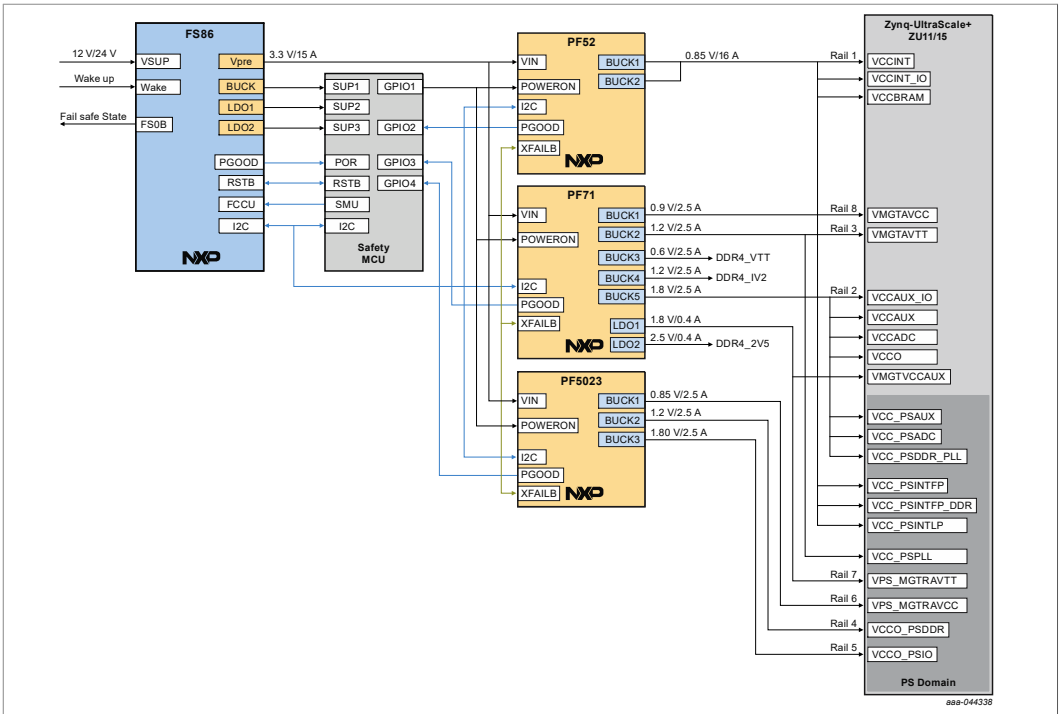

Figure 1. Typical NXP PMIC solution for ZU11 / ZU15 based system

Note: *In an actual application, the ZU11 or ZU15 Rail 1 current requirement may exceed 16 A, which is the PF52 maximum output current. If so, the customer must replace the PF52 with another power supply.*

2.2 PMIC configuration for ZU11 / ZU15

The FS86 pre-regulator Vpre output supplies input voltage to PF PMICs. PF71 contains five high efficiency buck converters and two regulators with load switch options. PF5023 contains three buck converters. PF52 is designed to be the primary core power supply. It contains two high power buck converters. Each buck converter in PF71 and PF5023 is rated up to 2500 mA, and each linear regulator is rated up to 400 mA. In the PF52, each buck converter is rated up to 8000 mA. Two buck converters configured as dual-phase can supply up to 16 A in total continuous output current. PF71, PF5023 and PF52 buck converters support Dynamic Voltage Scaling (DVS).

Table 1 summarizes the PMIC power supply configuration for ZU11 / ZU15.

An NXP Multi-PMIC internal power up sequencer can accurately implement power up and power down sequence synchronization for all power rails, using the PWRON and XFAILB functions of each NXP PMIC. The default sequence slots for PMICs are programmed via the OTP configuration registers. Each sequence slot includes time base and time slot information, allowing flexible power up / power down sequence configuration. This power up / power down sequencing in systems with ZU11 / ZU15 requirements is executed by the PMIC, and does not require control by the safety MCU.

Table 1. NXP PMIC output power configuration for ZU11 / ZU15

Xilinx ZU11 / ZU15 power rail		NXP PMIC output power configuration			
Rail	**Symbol**	**Output channel**	**Output voltage / V**	**Current capability / A**	**Power up sequence**

Table 1. NXP PMIC output power configuration for ZU11 / ZU15*...continued*

Xilinx ZU11 / ZU15 power rail		NXP PMIC output power configuration			
Rail 1	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR,VCCINT_IO, VCCBRAM	PF52	0.85	16	1
Rail 2	VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL,VCCAUX,VCCAUX_IO, VCCADC	PF71 BUCK5	1.8	2.5	2
Rail 3	VCC_PSPLL, VPS_MGTRAVTT	PF71 BUCK1	1.2	2.5	2
Rail 4	VCCO_PSDDR	PF5023 BUCK2	1.2	2.5	3
Rail 5	VCC_PSIO[0:3]	PF5023 BUCK3	1.8	2.5	3
Rail 6	VPS_MGTRAVCC	PF5023 BUCK1	0.85	2.5	2
Rail 7	VPS_MGTRAVTT, VMGTVCCAUX	PF71 LDO1	1.8	0.4	3
Rail 8	VMGTAVCC	PF71 BUCK2	2.5	0.4	1
NA	DDR4_1V2	PF71 BUCK4	1.2	2.5	3
NA	DDR4_VTT	PF71 BUCK3	0.6	2.5	3
NA	DDR4_2V5	PF71 LDO2	2.5	0.4	3

Note: *In an actual application, the ZU11 or ZU15 Rail 1 current requirement may exceed 16 A, which is the PF52 maximum output current. If so, the customer must replace the PF52 with another power supply.*

2.3 PMIC and Safety MCU interconnection

Table 2 details the IO connections between the Safety MCU and the PMIC.

Table 2. Xilinx ZU11 / ZU15 connection with PF52+PF71+PF5023

PMIC	Safety MCU	Block	Function
FS86 PGOOD	POR	IO	FS86 power good output, which connects to Safety MCU hardware reset
FS86 RESET	RESET		FS86 reset output, which connects to MCU software reset
FS86 FCCU	SMU		FS86 monitor MCU hardware fault
PF52&PF71&PF5023 POWERON	GPIO1		PF52, PF71, and PD5023 power on input request by MCU
PF52 PGOOD	GPIO2		PF52 power good indicator
PF71 PGOOD	GPIO3		PF71 power good indicator
PF5023 PGOOD	GPIO4		PF5023 power good indicator
PMIC I2C	I2C	Communication	SPI bus communication between PMIC and MCU

3 Functional safety

Functional safety is normally required for autonomous driving applications. One typical architecture, using ASIL-D and ASIL-B domains, is shown in Figure 2. In this architecture, an FS86 and a Safety MCU combine to form the ASIL-D domain, and a PF series PMIC with ZU11 / ZU15 form the ASIL-B domain.

The FS86 is an ASIL-D-ready PMIC, and PF52, PF71 and PF5023 are ASIL-B-ready. The NXP PMICs listed here are developed in compliance with the IOS26262 standard, and are appropriate for this architecture.

For customers who need a PF series PMIC with a ZU11 / ZU15 domain for ASIL-C or ASIL-D levels, the Extended Voltage Monitoring capability of the FS86 (VMONx) can be used to monitor and diagnose PMIC output voltage.

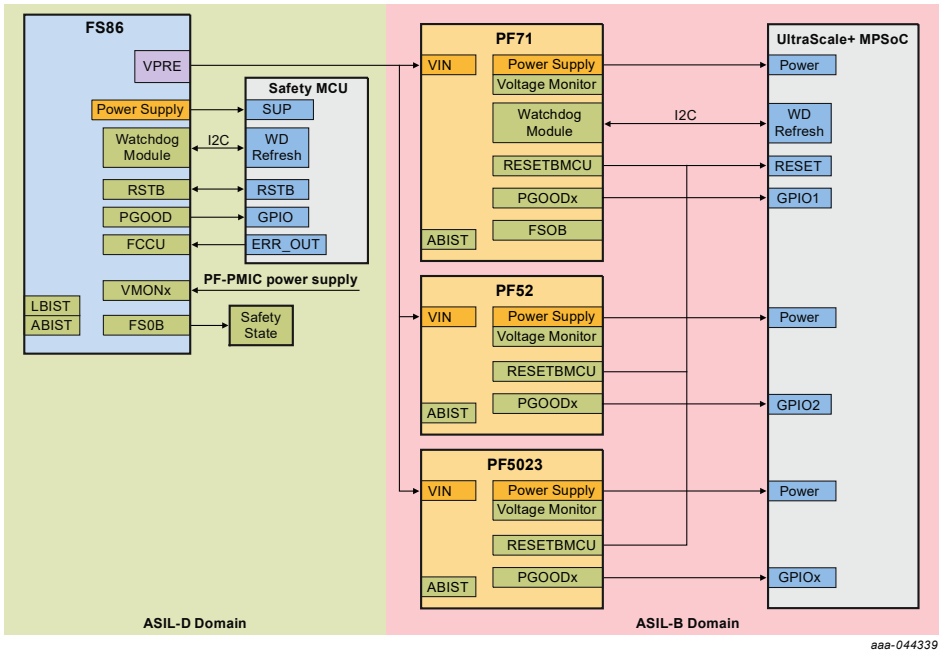

Figure 2. ASIL-D/B functional safety operation for Xilinx ZU11 / ZU15

The FS86 family and PF series devices implement embedded safety mechanisms that include these functional safety features:

- **Independent voltage monitoring and fault detection**: PMICs feature independent fault monitoring per regulator. Three types of faults, undervoltage (UV), overvoltage (OV), and current limit (ILIM), are monitored by the PMIC fault monitor block. The PMIC can indicate the output state per regulator through PGOOD.
- **I2C CRC and write protection**:*I2C secure write protection protects the secure registers against faulty operation using a dedicated safety mechanism.*
- **Analog built-in self-test (ABIST)**: When power to the system is turned on, the PMICs automatically test all output voltage monitors prior to the power up sequence. ABIST checks the state of the voltage monitoring block (OV/UV) per regulator, whether it's normal or not. If a failure on the OV/UV monitor is detected during ABIST, the PMIC will assert the corresponding ABIST flags.
- **VIN OVLO function**All NXP PMICs feature a Voltage In, Over Voltage Lockout (VIN_OVLO) circuit to monitor the main input supply of the PMIC. The PMIC monitors

its input voltage, and can initiate a power down sequence when a VIN_OVLO is detected in the system.

- **Functional safety output**: When a critical fault is detected by the PMIC, such as an incorrect regulator output or watchdog (WD) failure, the Fail-Safe Output 0 (FS0B) pin from FS86 is used to transition the system into a safe state.
- **Logic build-in self-test (LBIST, FS86 only):** LBIST verifies the correct functionality of the safety logic monitoring. FS86 performs LBIST after power on or upon wakeup from Standby mode.
- **External voltage monitor (FS86 only)**: The FS86 can monitor up to ten voltages, including FS86 supply rails or system PF device regulators. Depending on the safety requirements, voltage monitoring (VMON) can be used to monitor PF device(s), to reach the ASIL-D safety level for the system.
- **MCU failure monitoring (FS86 only)**: The FS86 features FCCU1/2, two input pins in charge of monitoring hardware failures of the safety MCU. Fault Collection and Control Unit (FCCU) pins can be connected to the Fault output I/O of MCU. When the FS86 detects a hardware failure from MCU through FCCU, the FS86 FS0B\RSTB pin can be asserted.
- **External IC monitoring (FS86 only)**: The FS86 features the ERRMON input pin, in charge of monitoring an external safety IC on the application.
- **Challenger watchdog monitoring (FS86 only)**: The challenger watchdog function is based on a question/answer strategy to monitor the safety MCU.

4 Schematics

Figure 3 to Figure 5 show MPSoC ZU11 / 15 application power solution schematics based on NXP PMICs.

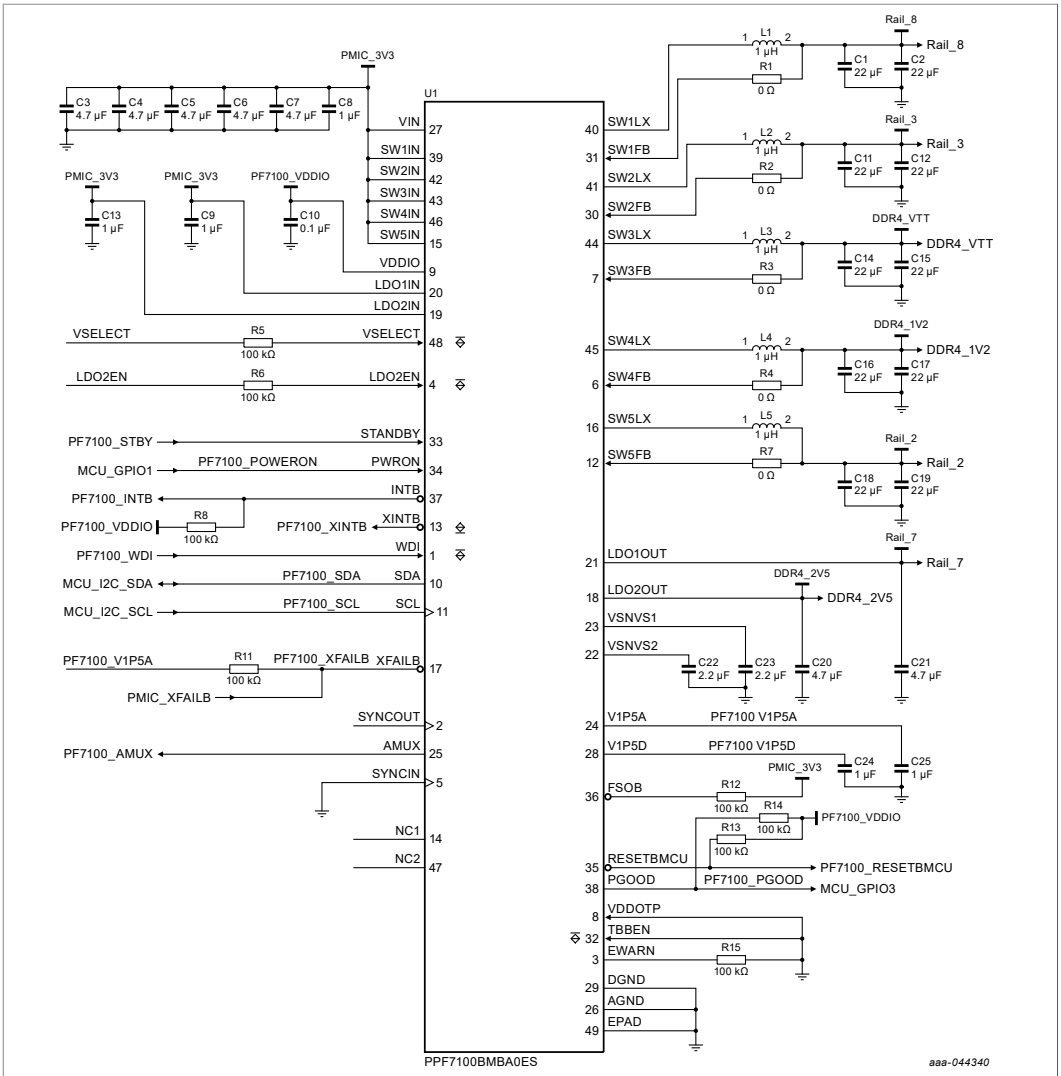

Figure 3. PF71 schematic for MPSoC ZU11 / 15 power rails

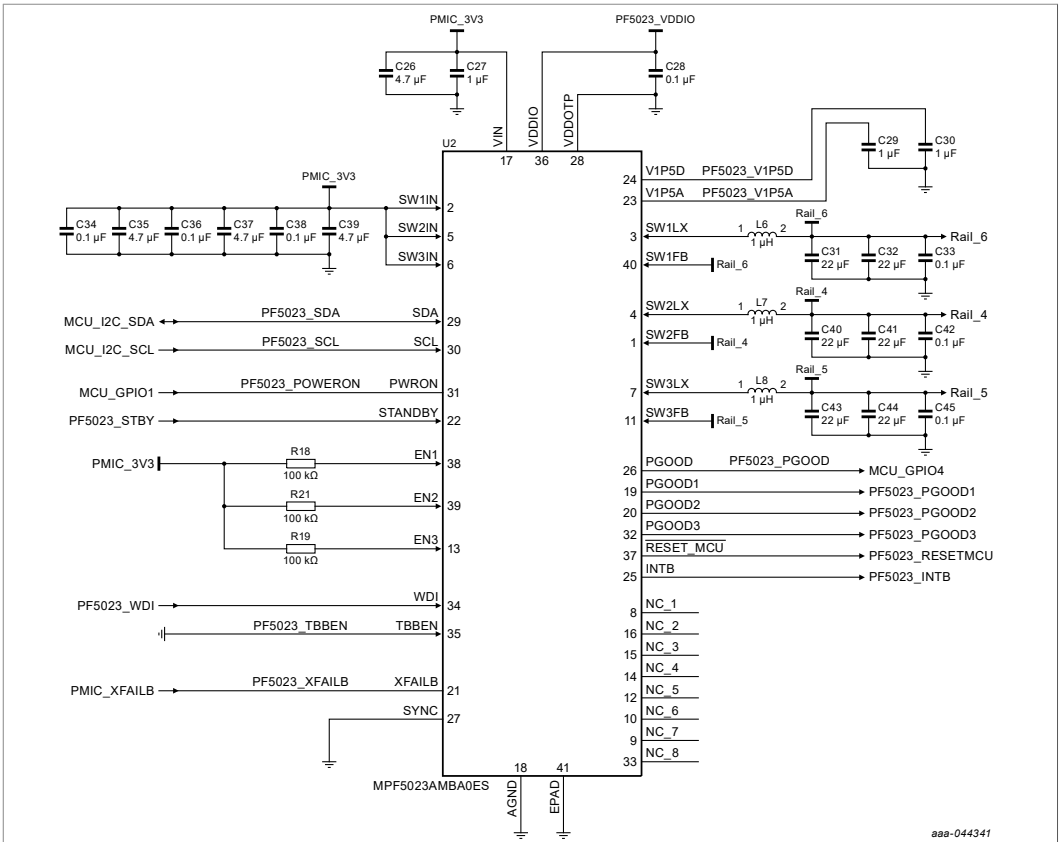

Figure 4. PF5023 schematic for MPSoC ZU11 / 15 power rails

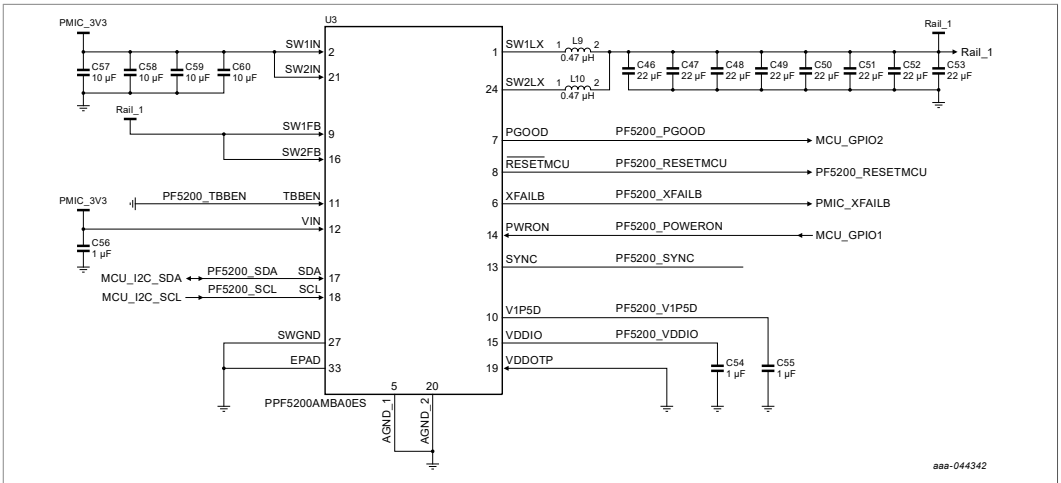

Figure 5. PF52 schematic for MPSoC ZU11 / 15 power rails

Bill of Materials

Table 3 provides a list of the recommended components on a ZU11 / 15 power solution with NXP PMICs. The components are listed with an example part number. Equivalent components may be used.

Table 3. ZU11 / 15 power solution bill of materials

Value	Qty	Part Number	Description	Vendor	Component
n/a	1	PF71	Power management IC	NXP	PMIC
n/a	1	PF5023	Power management IC	NXP	PMIC
n/a	1	PF52	Power management IC	NXP	PMIC
4.7 µF	11	GRM188C71C475KE21	CAP CER 4.7 µF 16 V 10% X7S 0603	MURATA	Input and Output capacitor
22 µF	24	GRT21BC81A226ME13	CAP CER 22 µF 10 V 20% X6S AEC-Q200 0805	MURATA	Input and Output capacitor
0.1 µF	8	GCM155R71C104KA55D	CAP CER 0.1 µF 16 V 10% X7R AEC-Q200 0402	MURATA	Filter capacitor
1 µH	8	TFM252012ALMA1R0MTAA	IND PWR 1.0 µH@1 MHZ 4.7 A 20% AEC-Q200 SMD	TDK	Buck inductor
0.47 µH	2	VCHA042A-R47MS6	IND PWR 0.47 µH@100 kHZ 10.6 A 20% AEC-Q200 SMD	CYNTEC	Buck inductor
1 µF	11	GCM155C71A105KE38D	CAP CER 1 µF 10 V 10% X7S AEC-Q200 0402	MURATA	Input capacitor
100 KΩ	11	CRCW0603100KJNEA	RES MF 100 KΩ 1/10 W 5% AEC-Q200 0603	VISHAY INTERTECHNOLOGY	Pull up resistor
10 µF	4	CGA4J1X7R0J106K125AC	CAP CER 10 µF 6.3 V 10% X7R AEC-Q200 0805	TDK	Input capacitor
0	5	ERJ-3GEY0R00V	RES MF ZERO OHM 1/10 W -- AEC-Q200 0603	PANASONIC	Short-circuit resistor
2.2 µF	2	GRT155C71A225KE13	CAP CER 2.2 µF 10 V 10% X7S AEC-Q200 0402	MURATA	Output capacitor

Resources

1. **PF5023 product summary page** https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/multi-channel-3-pmic-for-automotive-applications-3-high-power-fit-for-asil-b-safety-level:PF5023
2. **PF7100 product summary page** https://www.nxp.com/PF7100
3. **PF52 product summary page** https://www.nxp.com/PF5200
4. **FS86:** Engineering samples are ready. Customers can contact their NXP representatives to request documents and samples related to FS86. Also see https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-for-domain-controller-fit-for-asil-b-and-d:FS86
5. **Power Management community** https://community.nxp.com/community/Power-Management
6. **BYLink System Power Platform** https://www.nxp.com/BYLink

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