# AN13432

## NXP PMIC solution for XILINX UltraScale+ MPSoC ZU4 / ZU5 / ZU6 / ZU7 / ZU9 Processor

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**Document information**

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| Abstract | This AN presents two NXP PMIC solutions for powering Xilinx Zynq UltraScale+ MPSoC ZU4 / ZU5 / ZU6 / ZU7 / ZU9. One is a cost-optimized power solution with FS56 + PF81 + PF52, and one is a full performance power solution with FS86 + PF71 + PF5020 + PF52. |

**Revision history**

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| v.1 | 20211108 | Initial version |

# 1 Introduction

The Xilinx Zynq UltraScale+ MPSoC ZU4 / ZU5 / ZU6 / ZU7 / ZU9 is a high performance smart processing platform for deep learning. Its typical application is autonomous driving.

Designing a power solution for the full number of rails that delivers the full power required by the UltraScale+ MPSoC processor presents a challenge. The functional safety requirements make the power supply design even more complex, but an NXP flexible PMIC (Power Management IC) could be used to address this challenge, providing a total power solution for the ZU4 / ZU5 / ZU6 / ZU7 / ZU9 and system. This would simplify the design and save development time.

NXP PMICs have a built-in one-time programmable (OTP) memory that stores key startup configurations. Users can define the OTP configuration based on their application requirements. The PMIC also features a dedicated functional block for synchronizing multiple PMICs' power-up sequences, so an NXP Multi-PMIC arrangement can work like “one chipset” in the system. This means there is no need for an external controller for system default voltage configuration and power-up sequence configuration, which saves design effort and reduces the system complexity.

This AN introduces two typical NXP PMIC designs for ZU4 / ZU5 / ZU6 / ZU7 / ZU9 and related systems. Table 1 shows the power solutions. The detailed PMIC power tree configuration, power up sequence, and functional safety arrangements are described below. Customers could also change a PMIC's configuration based on their system requirements, thanks to NXP PMIC flexible configuration features which allow customized OTP definition.

**Table 1. Xilinx ZU4 / ZU5 / ZU / ZU7 / ZU9 power solutions**

| Power Supply Consolidation | Functional safety level | Power solution | |
|---|---|---|---|
| | | Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9 power supply | System power supply |
| Cost optimized power solution | QM | PF81 + PF52 | FS56 + PF81 + PF52 |
| Full performance power solution | ASIL-D / ASIL-B | PF71 + PF71 + PF5020 + PF52 | FS86 + PF71 + PF71 + PF5020 + PF52 |

# 2 Cost optimized power solution

A cost-optimized power solution is the target for always-on Functional Safety QM level applications. Table 2 defines one typical cost-optimized power solution with a PF81 and PF52 configuration to power ZU4 / ZU5 / ZU6 / ZU7 / ZU9. PF81 and PF52 are low voltage input PMICs. PF81 includes seven buck outputs and four low-dropout voltage regulator (LDO) outputs. PF52 has two bucks working in parallel to provide 16 A current. Each PF81 buck output current is 2.5 A maximum, and each of the LDO outputs supplies 0.4 A maximum.

Output voltages and power-up sequences for PF81 and PF52 are configured using OTP.

**Table 2. Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9 Cost-optimized power solution with PF81 + PF52**

| Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9 power rail | | PMIC output power configuration | | | |
|---|---|---|---|---|---|
| Rail | Symbol | Output channel | Output voltage / V | Current capability / A | Power-up sequence |
| Rail 1 | VCCINT, VCC_PSINTFP, VCC_PSINTLP,VCC_PSINTFP_DDR,VCCINT_IO, VCCBRAM | PF52 BUCK1 and 2 | 0.85 | 16 | 1 |
| Rail 2 | VCC_PSAUX,VCC_PSADC, VCC_PSDDR_PLL,VCCAUX,VCCAUX_IO, VCCADC | PF81_BUCK7 | 1.8 | 2.5 | 2 |
| Rail 3 | VCC_PSPLL, VMGTAVTT | PF81_BUCK4 | 1.2 | 2.5 | 2 |
| Rail 4 | VCCO_PSDDR | PF81_BUCK5 | 1.2 | 2.5 | 3 |
| Rail 5 | VCC_PSIO[0:3] | PF81_LDO3 | 1.8 | 0.4 | 3 |
| Rail 6 | VPS_MGTRAVCC | PF81_BUCK1 | 0.85 | 2.5 | 2 |
| Rail 7 | VPS_MGTRAVTT, VMGTVCCAUX | PF81_LDO2 | 1.8 | 0.4 | 3 |
| Rail 8 | VPS_MGTRAVCC | PF81_BUCK3 | 0.9 | 2.5 | 2 |
| Rail 9 | VCCINT_VCU | PF81_BUCK2 | 0.9 | 2.5 | 1 |
| NA | VTT(DDR) | PF81_BUCK6 | 0.6 | 2.5 | 3 |
| NA | VPP(DDR) | PF81_LDO1 | 2.5 | 0.4 | 3 |

***Note:*** *In actual applications, the ZU6 / ZU7 / ZU9 Rail 1 current requirement may exceed 16 A, which is the PF52 maximum output current. If so, the customer must replace the PF52 with another power supply.*

For a real automotive application with ZU4 / ZU5 / ZU6 / ZU7 / ZU9 for autonomous driving, normally a microcontroller unit (MCU) is needed. Figure 1 shows an NXP PMIC solution using FS56 + PF81 to power an MCU+ UltraScale + MPSoC system. FS56 is a high-voltage PMIC that supports a 12 V battery system in a vehicle. FS56 includes two buck outputs. One buck output can power the MCU, and the other one can power PF81 + PF52. The MCU configures FS56, PF81, and PF52 registers through I2C. FS56 and PF81 each have a “PGOOD” (power good) pin to indicate to the MCU whether the PMIC power supply output is within specification. The MCU controls the power-on request for PF81 and PF52 using the PMIC PWRON pin.

This design's combination of FS56, PF81 and PF52 supports QM level safety. NXP also offers pin-to-pin (P2P) compatible ASIL-B level devices.

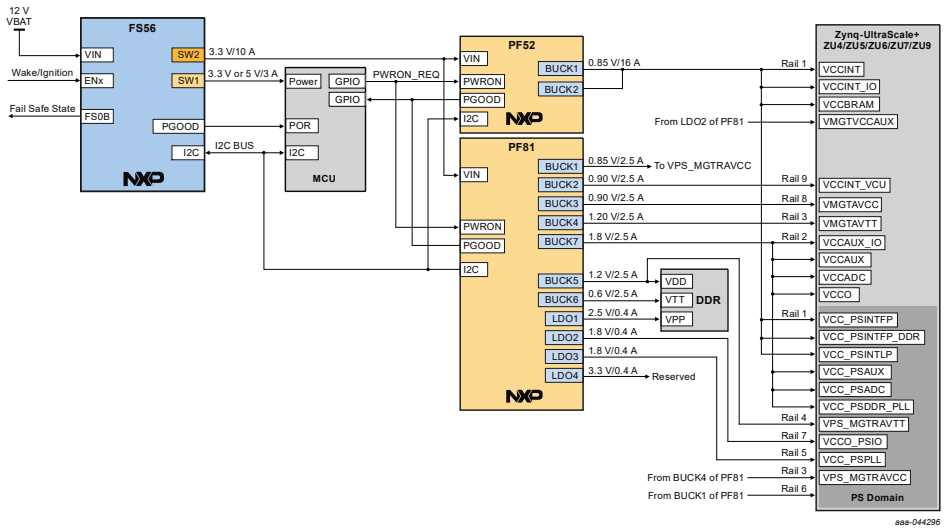


**Figure 1. Cost optimized system power solution with FS56 + PF81 + PF52**

# 3 Full performance power solution

The full performance power solution is designed for systems where low-power mode is required, or where autonomous driving applications require functional safety. Some applications with ZU4 / ZU5 / ZU6 / ZU7 / ZU9 require ultra-low-power, reduced functional states to maximize battery life or reduce overall power consumption. This full performance power solution is designed for functional safety ASIL-D / B applications. The FS86 + 2*PF71 + PF5020 + PF52 PMIC solution provided here facilitates a power solution design for a ZU4 / ZU5 / ZU6 / ZU7 / ZU9 based system.

## 3.1 Power solution

Table 3 defines a 2 * PF71 + PF5020 + PF52 power supply configuration for Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9. PF71 contains five high-efficiency buck converters and two LDOs with load switch options. PF5020 contains three bucks and one LDO.

Each buck converter in the PF71 + PF5020 part of the solution is rated up to 2.5 A, and each linear regulator is rated up to 0.4 A. PF52 has two bucks that could work in parallel to provide a 16 A current.

This power solution uses a dedicated regulator for the UltraScale+ MPSoC power rail. The use of a dedicated voltage regulator per rail, even when rails have the same voltage level, allows a rail or rails to be shut down to save power consumption.

**Table 3. Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9 Full performance power solution with 2 * PF71 + PF5020 + PF52**

| Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9 power rail | | PMIC output power configuration | | | |
|---|---|---|---|---|---|
| Rail | Symbol | Output channel | Output voltage / V | Current capability / A | Power-up sequence |
| Rail 1 | VCC_PSINTLP | PF71_2_BUCK1 | 0.85 | 2.5 | 1 |
| Rail 2 | VCC_PSAUX, VCC_PSADC | PF71_2_BUCK2 | 1.8 | 2.5 | 2 |
| Rail 3 | VCC_PSPLL | PF71_2_LDO1 | 1.2 | 0.4 | 2 |

**Table 3. Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9 Full performance power solution with 2 * PF71 + PF5020 + PF52*...continued***

| Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9 power rail | | PMIC output power configuration | | | |
|---|---|---|---|---|---|
| **Rail** | **Symbol** | **Output channel** | **Output voltage / V** | **Current capability / A** | **Power-up sequence** |
| Rail 4 | VCC_PSIO[0:3] | PF71_2_LDO2 | 1.8 | 0.4 | 3 |
| Rail 5 | VCC_PSINTFP, VCC_PSINTFP_DDR | PF71_1_BUCK1&2 | 0.85 | 5 | 1 |
| Rail 6 | VCC_PSDDR_PLL | PF5020_LDO1 | 1.8 | 0.4 | 2 |
| Rail 7 | VCCO_PSDDR | PF71_2_BUCK3 | 1.2 | 2.5 | 3 |
| Rail 8 | VCCINT,VCCINT_IO,VCCBRAM | PF52 BUCK1&2 | 0.85 | 16 | 1 |
| Rail 9 | VCCAUX,VCCAUX_IO,VCCADC | PF5020_BUCK3 | 1.8 | 2.5 | 2 |
| Rail 10 | VPS_MGTRAVCC | PF5020_BUCK1 | 0.85 | 2.5 | 2 |
| Rail 11 | VPS_MGTRAVTT | PF5020_BUCK2 | 1.8 | 2.5 | 3 |
| Rail 12 | VMGTAVTT | PF71_1_BUCK5 | 1.2 | 2.5 | 2 |
| Rail 13 | VMGTAVCC | PF71_1_BUCK4 | 0.9 | 2.5 | 2 |
| Rail 14 | VMGTAVCCAUX | PF71_1_LDO1 | 1.8 | 0.4 | 2 |
| Rail 15 | VCCINT_VCU | PF71_1_BUCK3 | 0.9 | 2.5 | 1 |
| NA | VTT(DDR) | PF71_2_BUCK3 | 0.6 | 2.5 | 3 |
| NA | VPP(DDR) | PF71_2_BUCK5 | 2.5 | 2.5 | 3 |

***Note:*** *In an actual application, the ZU6 / ZU7 / ZU9 Rail 8 current requirement may exceed 16 A, which is the PF52 maximum output current. If so, the customer must replace PF52 with another power supply.*

Figure 2 demonstrates a typical architecture for an autonomous driving ECU that requires functional safety. The FS86 + ASIL-D MCU is the ASIL-D domain for the Decision and Control function. The PF71 + PF5020 + PF52 powers the UltraScale+ MPSoC in the ASIL-B domain. FS86 is a high-voltage PMIC that supports a 12 V or 24 V battery system. It is designed to meet the power and security requirements of an ASIL-D MCU. The FS86 has multiple outputs to power an MCU and its peripherals, like CAN, Ethernet, and Memory. The FS86 can also provide input power to a low voltage PMIC through Vpre. PF71, PF5020 and PF52 are appropriate for use in ASIL-B designs. Both PMICs in this solution have integrated functional safety features, significantly reducing system functional safety development efforts.

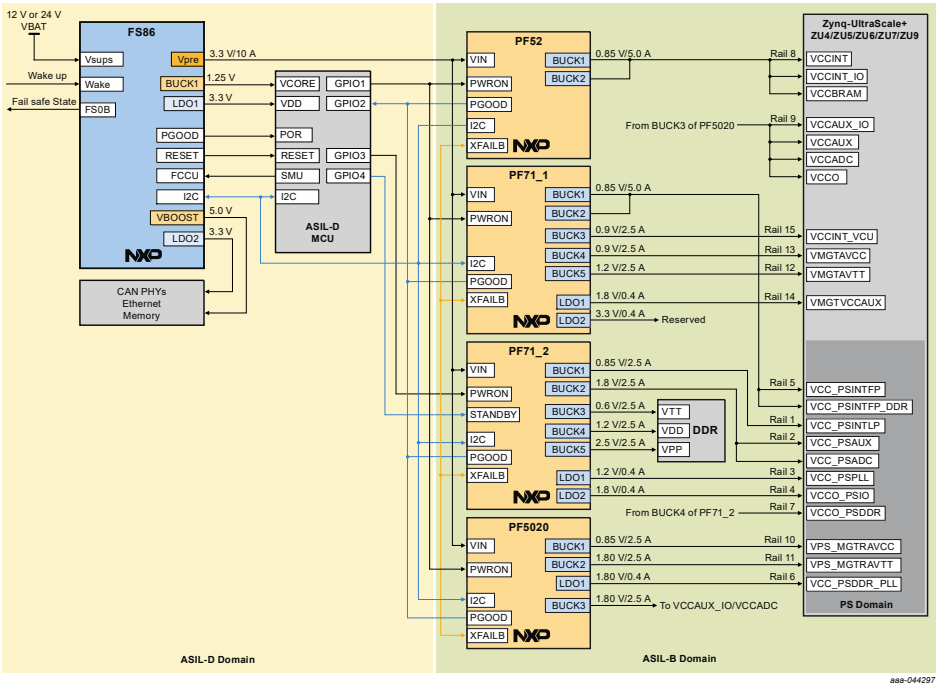


**Figure 2. Full performance system power solution with FS86+PF52+PF71+PF5020**

***Note:*** *In an actual application, the ZU6 / ZU7 / ZU9 Rail 8 current requirement may exceed 16 A, which is the PF52 maximum output current. If so, the customer must replace PF52 with another power supply.*

Table 4 details the IO connections between PMICs and ASIL-D MCUs. PF71, PF5020, or PF52 power-on is triggered by the ASIL-D MCU using the PMIC PWRON pin. These combinations could act as öne PMIC through the NCP PMIC internal power-up sequencer, PWRON, XFAILB function. This multiple PMIC scheme effectively implements accurate power-up and power-down sequence synchronization for all power rails using only PMICs, without the need for MCU control.

**Table 4. Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9 connection with FS86 + PF52 + PF71 + PF5020**

| PMIC | ASIL-D MCU | Block | Function |
|---|---|---|---|
| FS86 PGOOD | POR | IO | FS86 power good output which connect to MCU hardware reset |
| FS86 RESET | RESET | | FS86 reset output which connect to MCU software reset |
| FS86 FCCU | SMU | | FS86 monitor MCU hardware fault |
| PF52, PF71_1, and PF5020 PWRON | GPIO1 | | PF52, PF71_1, and PF5020 power on input request by MCU |
| PF52, PF71, and PF5020 PGOOD | GPIO2 | | PF52&&PF71&PF5020 power good indicator |
| PF71_2 PWRON | GPIO3 | | PF71_2 power-on input request by MCU |
| PF71_2 STANDBY | GPIO4 | | PF71_2 standby mode input request by MCU |
| FS86, PF52, PF71, and PF5020 I2C | I2C | Communication | I2C bus communication for FS86, PF52, PF71, and PF5020 |

## 3.2 Functional safety

NXP PMICs are developed in compliance with the ISO26262 standard.

The FS86, PF71, PF5020, and PF52 devices implement embedded safety mechanisms that include these functional safety features:

- **Independent voltage monitoring and fault detection**: PMICs feature independent fault monitoring per regulator. Three types of faults, Under Voltage (UV), Over Voltage (OV), and Current Limit (ILIM), are monitored by the PMIC fault monitor block. The PMIC can indicate the output state per regulator through PGOOD.
- **I2C CRC and write protection**: I2C secure write protection protects the secure registers using a dedicated safety mechanism.
- **Analog built-in self-test (ABIST)** When power to the system is turned on, the PMICs automatically test all output voltage monitors prior to the power-up sequence. ABIST checks the state of the voltage monitoring block (OV/UV) per regulator, whether it is normal or not. If a failure on the OV/UV monitor is detected during ABIST, the PMIC will assert the corresponding ABIST flags.
- **Functional safety output**: When a critical fault is detected by the PMIC, such as an incorrect regulator output or Watchdog (WD) failure, the FS0B pin from FS86 is used to transition the system into a safe state.
- **Logic build-in self-test (LBIST, FS86 only):** LBIST verifies the correct functionality of the safety logic monitoring. FS86 performs LBIST after power on or upon wakeup from Standby mode.
- **External voltage monitor (FS86 only)**: The FS86 can monitor up to ten voltages, including FS86 supply rails or system PF device regulators. Depending on the safety requirements, voltage monitoring (VMON) can be used to monitor PF devices, to reach the ASIL-D safety level for the system.
- **MCU failure monitoring (FS86 only)**: The FS86 features FCCU1/2, two input pins in charge of monitoring hardware failures of the safety MCU. FCCU pins can be connected to the Fault output I/O of MCU. When FS86 detects a hardware failure from MCU through FCCU, the FS86 FS0B / RSTB pin can be asserted.
- **External IC monitoring (FS86 only)**: The FS86 features the Error Monitoring (ERRMON) input pin, in charge of monitoring an external safety IC on the application.
- **Challenger watchdog monitoring (FS86 only)**: The challenger Watchdog function is based on a question/answer strategy to monitor the safety MCU.

Figure 3 shows the functional safety related signal configuration based on ASIL-D / B safety requirements for ZU4 / ZU5 / ZU6 / ZU7 / ZU9 system applications.

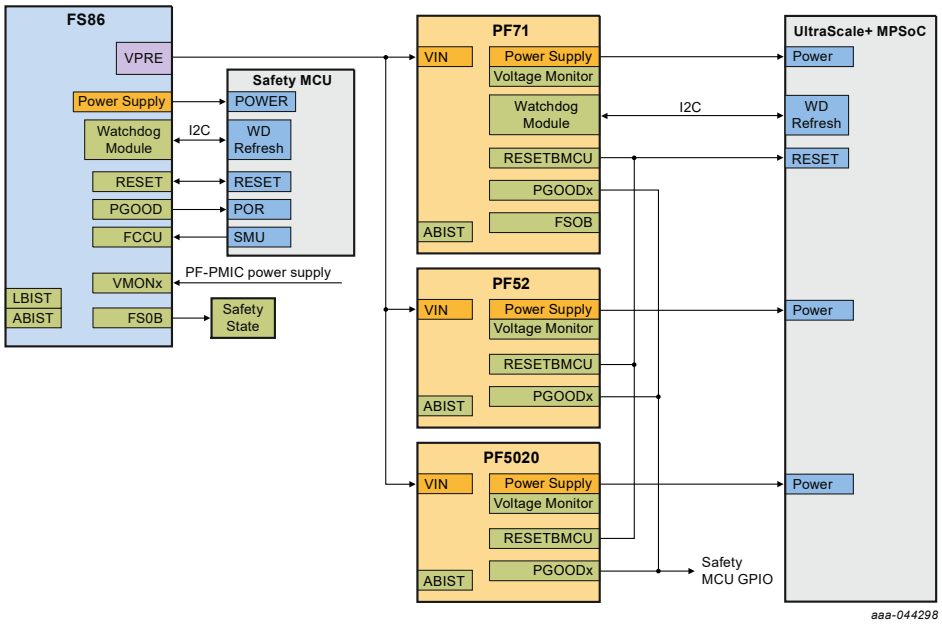


Figure 3. ASIL-D / B functional safety operation for Xilinx ZU4 / ZU5 / ZU6 / ZU7 / ZU9

# 4 Reference Resources

[1] FS86 overview

[2] FS56 webpage includes documentation and tools (Datasheet, Safety Manual, FMEDA, SW driver)

[3] PF81 webpage includes documentation and tools (Datasheet, Safety Manual, FMEDA, SW driver)

[4] PF71 webpage includes documentation and tools (Datasheet, Safety Manual, FMEDA, SW driver)

[5] PF5020 webpage includes documentation and tools (Datasheet, Safety Manual, FMEDA, SW driver)

[6] PF52 overview

[7] Power Management Community

[8] BYLink System Power Platform

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