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How to Enable Spread Spectrum for RT Family
Rev. 2 — 25 August 2023   **Application note**

Document Information

Information	Content
Keywords	i.MX RT, i.MX RT Crossover MCUs, spread spectrum, communication technology, frequency spectrum, transmission signal, bandwidth, wireless communication, electromagnetic interference, EMI, EMI performance, System-on-Chip, SoC, application processors
Abstract	This document intends to introduce the basic theory about spread spectrum and how to enable this feature for i.MX RT feature in order to enhance EMI performance.

1 Background

Spread spectrum is a communication technology that turns the frequency spectrum of a transmission signal to a wider bandwidth than its original bandwidth. It is widely used in the field of wireless communication.

This document introduces the basic theory about the spread spectrum and how to enable this feature for RT feature to enhance Electro Magnetic Interference (EMI) performance.

2 Spread spectrum introduction

- **Narrowband signals**
  The narrowband signals have the signal strength concentrated, as shown in Figure 1. A narrowband signal (or in this case the system clock) has a spectrum signature of a sharp narrow peak centered on a specific frequency.
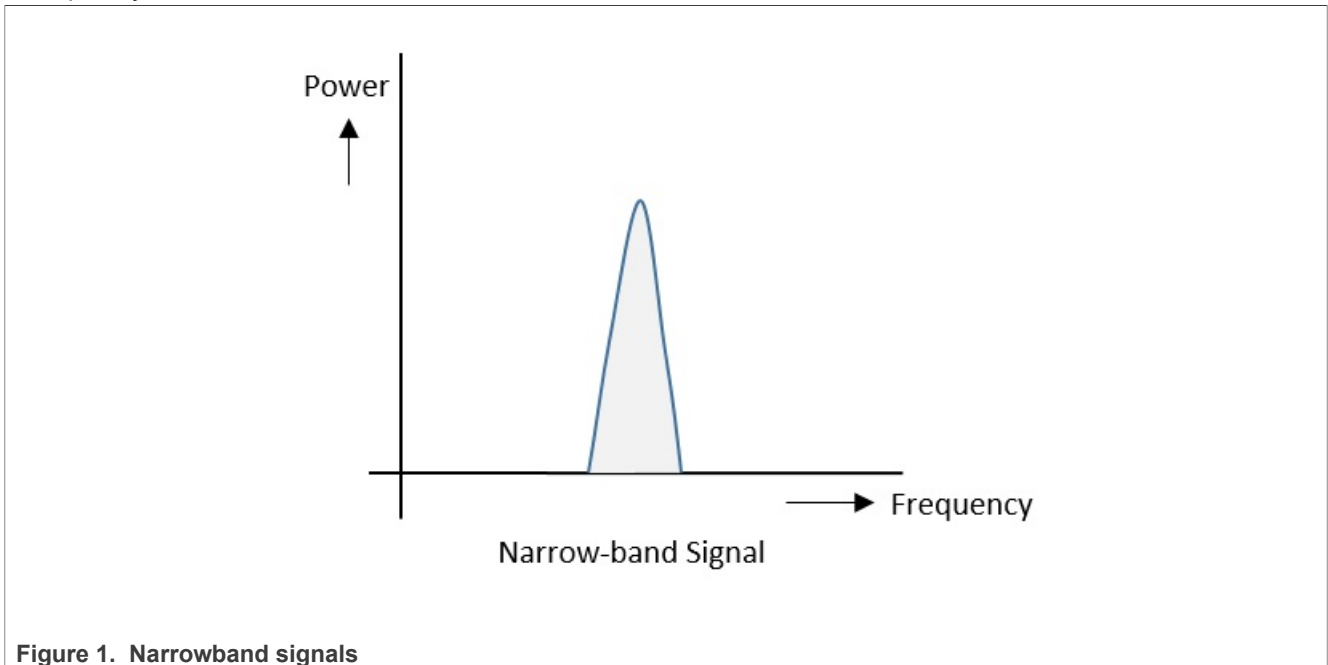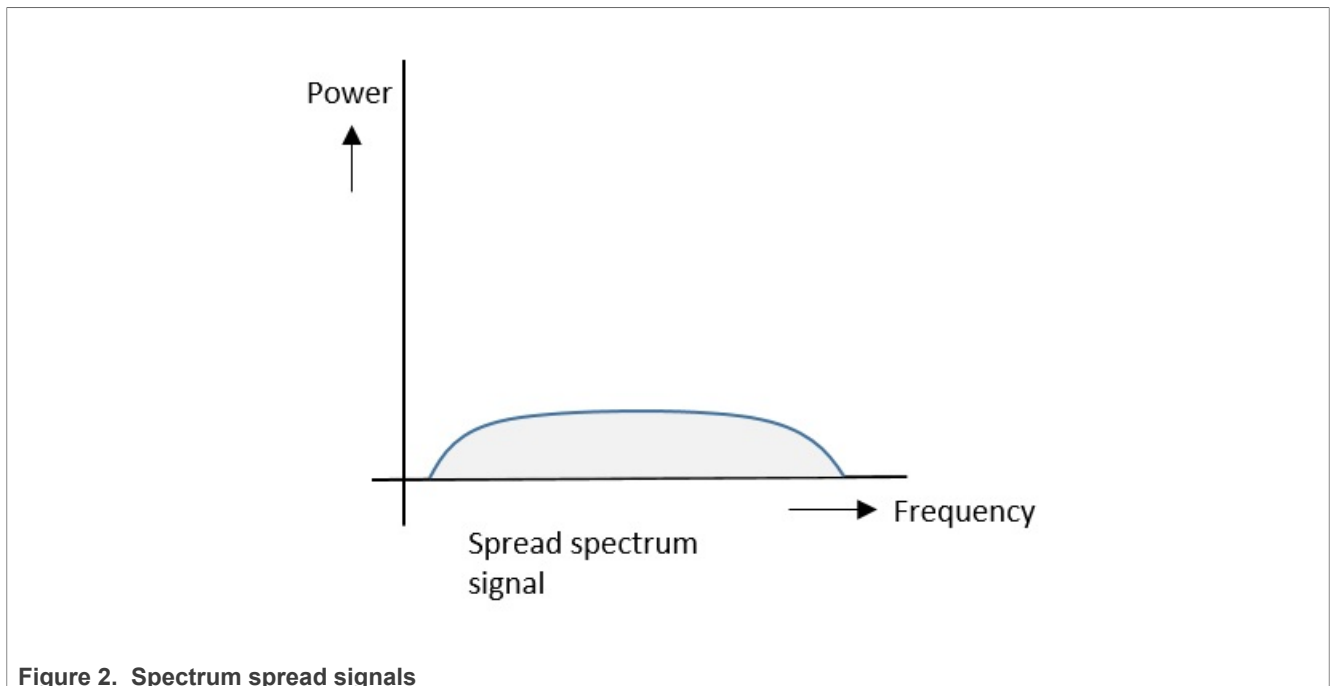

Figure 1. Narrowband signals

Some characteristics are as follows:
  – The band of signals occupies a narrow range of frequencies.
  – The power density is high.
  – The spread of energy is low and concentrated.
- **Spread spectrum signals**
  The spread spectrum signals have the signal strength distributed, as shown in Figure 2.
  Instead of keeping the narrowband signal (or system clock in our case) at a fixed frequency, the spread spectrum works by moving the frequency across a defined range. The result is that the energy peak gets reduced and spreads over a range of frequency values.

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Figure 2. Spectrum spread signals

Some characteristics are as follows:

– The band of signals occupies a wide range of frequencies.

– The power density is low.

– The energy is wide spread.

From the above descriptions, you can see that with these characteristics, the spread spectrum signals are highly resistant to interference or jamming.

3 Spread spectrum configuration

For the RT family, the `SYS_PLL2`, `AUDIO_PLL`, and `VIDEO_PLL` support the spread spectrum (spread down). To enable the spread spectrum function, configure registers in SDK as shown in below.

```
/*
    0x40c84260 is used to configure the value of
    STOP(bit[31-16]) and STEP(bit[14:0]). Bit 8
    is the enable bit.
    The Frequency change is:
        Frequency change = STOP/B *24MHz

    The Step value is :
        The max frequency change for each time = STEP/B * 24Mhz

    0x40c842a0 is used to configure the value of B.

    So that, the following configure is:
    STOP = 0x4B0;
    B = 0x960;
    STEP = 0x6;
    Frequency change = 12MHz
    The max frequency change for each time = 6OKHz

    STOP = 0x258;
    B = 0x960;
```

```
    STEP = 0x6;
    Frequency change = 6MHZ

    The max frequency change for each time = 60KHz
*/
    *(uint32_t *)(0x40c84260) = 0x04B08006; //12MHz
    //*(uint32_t *)(0x40c84260) = 0x02588006; //6MHZ
    *(uint32_t *)(0x40c842a0) = 0x00000960;


/*! @brief Spread specturm configure Pll */
typedef struct _clock_pll_ss_config
{
    uint16_t stop; /*!< Spread spectrum stop value to get frequency change. */
    uint16_t step; /*!< Spread spectrum step value to get frequency change step.
 */
} clock_pll_ss_config_t;

/*! @brief PLL configure for Sys Pll1 */
typedef struct _clock_sys_pll1_config
{
    bool pllDiv2En;             /*!< Enable Sys Pll1 divide-by-2 clock or not. */
    bool pllDiv5En;             /*!< Enable Sys Pll1 divide-by-5 clock or not. */
    clock_pll_ss_config_t *ss; /*!< Spread spectrum parameter,
                                    it can be NULL, if ssEnable is set to false */
    bool ssEnable;              /*!< Enable spread spectrum flag */
} clock_sys_pll1_config_t;
```

The following Phase Locked Loop (PLL) in RT1xxx series supports the spread spectrum.

Table 1. PLL in RT1xxx series

PLL	RT1170	RT1010	RT1015	RT1020/1024	RT1050	RT1060/1064
PLL528	✓	✓	✓	✓	✓	✓
PLL_528_PFDn	✓	✓	✓	✓	✓	✓
Audio_PLL	✓	NA	NA	NA	NA	NA
Video_PLL	✓	NA	NA	NA	NA	NA
PLL_1G	✓	NA	NA	NA	NA	NA

There are two points when enabling the spread spectrum: Spread spectrum range and Step.

- The spread range indicates how much frequency the PLL sweeps down. For example, a spread range of 6 MHz indicates that the PLL sweeps from **Target_frequency** to **Target_Frequency - 6 MHz** and then sweeps back.
  The basic formula is used to calculate the range:

$$\text{Range} = \text{STOP}\big/\text{B} * 24\text{MHz} \tag{1}$$

- The spread step indicates how many frequencies are changed in one step.
  The basic formula is used to calculate the step:

$$\text{Step} = \text{STEP}\big/\text{B} * 24\text{MHz} \tag{2}$$

Taking PLL528 as an example:

- STOP = 0x4B0
- B = 0x960

- STEP = 0x6

Then the Range and Step are:

- Range: 12 MHz
- Step: 60 kHz

The PLL528 sweeps from 528 MHz to 516 MHz (528 - Range) and sweeps back with one step 60 kHz.

STOP, **B**, and **STEP** can be configured in `SYS_PLL2_SS` and `SYS_PLL2_MFD` registers on RT10xx series.

STOP, **B**, and **STEP** can be configured in `CCM_ANALOG_PLL_SYS_SS` and `CCM_ANALOG_PLL_SYS_DENOM` registers on RT1170.

Now when a PLL is initialized, the spread spectrum function can also be configured. Fill the **STOP**, **B**, and **STEP** and then initialize the PLL. Once the PLL is enabled, the spread spectrum function is also enabled.

4   Radiation comparison under spread spectrum

MIMXRT1170-EVK platform is used for such test. The radiation value is tested under different configuration for spread spectrum using noncontact probe and spectrum analyzer.

From the settings of the test result, 6 MHz and 12 MHz stop value is recommended in such case to improve EMI performance.

Table 2. Test result under different spread spectrum configuration

Spread spectrum (Hz)	0.75 M	1.5 M	3 M	6 M	12 M	24 M	--->	6 M and 12 MHz configuration is recommended.
Test result (dBm)	-46.2	-46.56	-49.85	-52.31	-53.35	-54.3		

Figure 3. Spectrum under 3 MHz configuration

Figure 4. Spectrum under 6 MHz configuration

5 Reliability test under spread spectrum

The Synchronous DRAM (SDRAM) reliability is verified under the spread spectrum enabled on the MIMXRT1170-EVK platform.

Table 3 describes the test pattern.

Table 3. Basic configuration of the test

	Module	Frequency
Core	Cortex-M7	996 MHz
AXI to SEMC	32 bit	240 MHz
SEMC	32 bit	198 MHz
SDRAM chip	w9825g6kh	256 Mb/up to 200 MHz
L1 Dcache	Total 32 KB/One-line 32 B	—
Code	Text region in ITCM Data region in DTCM CStack region in DTCM	—

From the test result, both 6 MHz and 12 MHz spread spectrum configuration can pass the stress test under full temp test. The result indicates that it is reliable to enable the spectrum spread feature for SDRAM clock.

```
DRAM test setting:
                Base Address: 0x80000000;
                Test Size: 67108864 Bytes;
                Test Loop: 1;
                DRAM Freq: 198010624;
                Fail Stop: 0;
                Enable Cache: 0;
                Core clock: 996056064;
                AHB clock: 120006784;
                SEMC clock: 198010624;


memtester version 4.3.0 (32-bit)
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want 64MB (67108864 bytes)
Loop 1/1:
  Stuck Address: ok
  Random Value: ok
  Compare XOR: ok
  Compare SUB: ok
  Compare MUL: ok
  Compare DIV: ok
  Compare OR: ok
  Compare AND: ok
  Sequential Increment: ok
  Solid Bits: ok
  Block Sequential: ok
  Checkerboard: ok
  Bit Spread: ok
  Bit Flip: ok
  Walking Ones: ok
  Walking Zeroes: ok
  8-bit Writes: ok
  16-bit Writes: ok

Done and Passed!
exit_code 0x0
```

Figure 5. Reliability test result

6 SEMC timing configuration under spectrum spread

Considering about Smart External Memory Controller (SEMC) timing configuration under the spectrum spread, check the following points:

- For more stability of SDRAM, the SEMC timing configuration can be set with bigger margin based on the working clock speed.
- Referring to Table 4, the minimum values of tRC, $tRAS$, tRP, $tRCD$, tRW, and $tRRD$ can be set more one or two cycles in SEMC register SDRAMCR1 and SDRAMCR2. For example, the tRC is 6 cycles (60 ns minimum at 166 MHz) for standard. We can set it to **7** (or **8**) cycles under spectrum spread mode.
- For $tREF$ (Refresh Cycle Time), it is set smaller than the maximum refresh cycle (64 ms). This setting can be implemented in SEMC register SDRAMCR3. In NXP SDK, the $tREF$ is set to be lower than half of the maximum refresh cycle.
- For the detailed SEMC timing configurations, refer to the NXP SDK.

Table 4. SDRAM device timing

Symbol	Parameter	Minimum	Maximum	Minimum	Maximum	Unit
t_{RC}	Command period (REF to REF/ACT to ACT)	60	—	60	—	ns
t_{RAS}	Command period (ACT to PRE)	42	100 K	37	100 K	ns
t_{RP}	Command period (PRE to ACT)	18	—	15	—	ns
t_{RCD}	Active command To read/write command delay time	18	—	15	—	ns
t_{RRD}	Command period (ACT [0] to ACT[1])	12	—	14	—	ns
t_{DPL}	Input data to precharge command delay time	12	—	14	—	ns
t_{DAL}	Input data to active/refresh command delay time (during auto-precharge)	30	—	30	—	ns
t_{MRD}	Mode register program time	12	—	14	—	ns
t_{DDE}	Power down exit setup time	6	—	7	—	ns
t_{XSR}	Exit self-refresh to active time (4)	66	—	70	—	ns
t_T	Transition time	0.3	1.2	0.3	1.2	ns
t_{REF}	Refresh cycle time (8192)					
	$T_a <= 70\ ^oC$ Com.,Ind., A1, A2	—	64	—	64	ms
	$T_a <= 85\ ^oC$,Ind., A1, A2	—	64	—	64	ms
	$T_a <= 85\ ^oC$ A2	—	32	—	32	ms

7 Performance test under spread spectrum

The performance test is done under spectrum spread, check below test environment and test result. It can conclude that spectrum spread has small impact to SDRAM R/W performance and has no impact to applications.

- Project configuration: `sdram_debug`
- SDRAM MPU configuration: non-shareable/cacheable/wb/disable Dcache
- Four test environments: Initial, 6 MHz, 12 MHz, and 24 MHz
- Test results: Test 16 kbit and 32 kbit data write/read performance for a few seconds. The results show that the read performances are all 22 MB/s. The write performances are as shown in Figure 6.

Table 5. SDRAM performance test under spread spectrum

		Initial	6 M	12 M	24 M
Average write	Perf (MB/s)	693	689	685	677
	Reduction percentage	—	-0.6%	-1.2%	-2.3%

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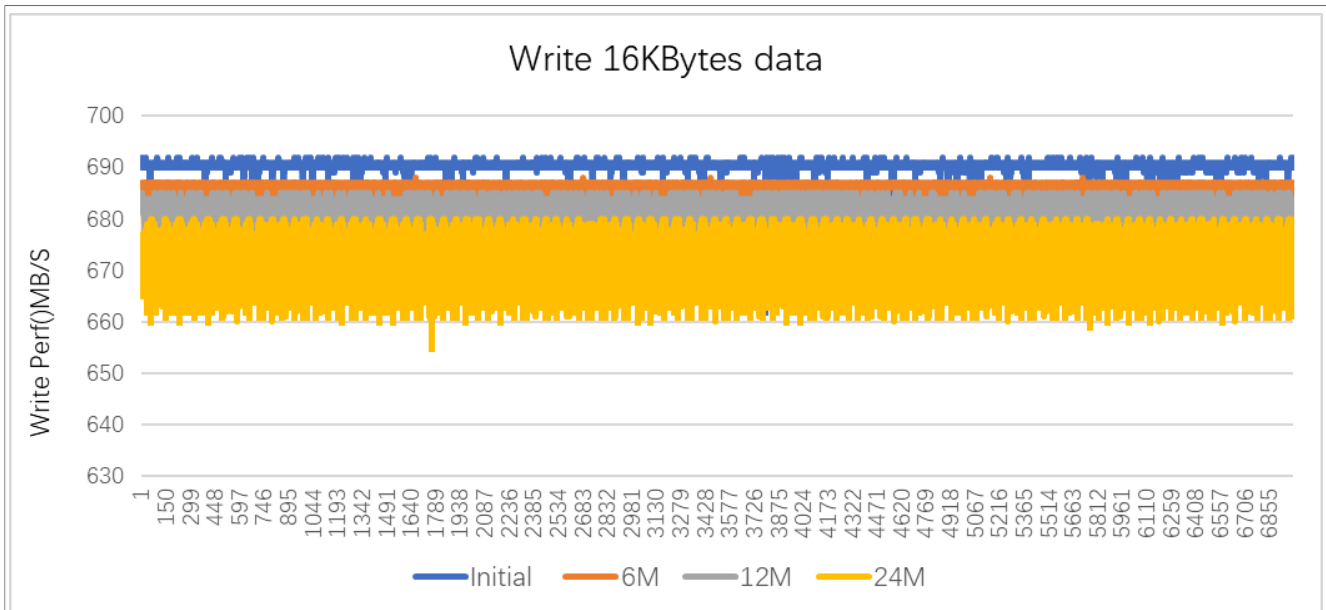
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Figure 6. SDRAM performance test under spread spectrum

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9 Revision history

Table 6 summarizes the revisions to this document.

Table 6. Revision history

Revision number	Release date	Description
2	25 August 2023	Updated Section 3
1	09 March 2021	Updated Section 3
0	June 2020	Initial public release

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