

## i.MX RT1170: 1 GHz Crossover MCU with Arm® Cortex® Cores

## i.MX-RT1170

Last Updated: Apr 11, 2024

i.MX RT1170 Crossover MCUs are dual-core devices featuring an Arm® Cortex®-M7 and Arm® Cortex®-M4 for real-time microcontroller (MCU) performance and high integration for automotive, industrial and IoT applications.

The i.MX RT1170 CM7 operates at up to 1 GHz and the CM4 up to 400 MHz with 2 MB on-chip RAM. The real-time microcontroller (MCU) family offers various memory interfaces and a wide range of connectivity interfaces including 3x Ethernet up to Gbps with TSN/AVB, UART, SPI, I<sup>2</sup>C, USB and 3x CAN FD. The i.MX RT1170 provides advanced embedded security including secure boot and crypto engines.

The i.MX RT1170 family is supported by the MCUXpresso ecosystem, which includes an SDK, a choice of IDEs and secure provisioning and configuration tools to enable rapid development.

## i.MX RT1170 Crossover MCU Block Diagram

| System Control                               | Main CPU Platform  |                                 | Connectivity              |                   |                    |                          |  |
|--|--|---------------------------------|---------------------------|-------------------|--------------------|--------------------------|--|
| DC-DC and LDO                                | Arm® Cortex®-M7 (up to 1 GHz)  |                                 | ASRC                      |                   | GPIO               |                          |  |
| DC-DC and LDC                                | 32 KB D-cache w/ ECC 3   | 2 KB I-cache w/ ECC<br>NVIC     | 3 x (                     | CAN-FD            |                    | HS GPIO                  |  |
| 2 x eDMA                                     | Up to 512 KB TCM w/ ECC  |                                 | 8-ch                      | 8-ch. DMIC        |                    | 6 x I <sup>2</sup> C     |  |
| Message Unit                                 | Secondary CPU Platform   |                                 | 2 x e                     | 2 x eMMC/SD       |                    | 4 x I <sup>2</sup> S/SAI |  |
|  | Arm Cortex-M4 (up to 400 MHz)  |                                 | 2 x E                     | 2 x EMVSIM        |                    | 8 x 8 Keypad             |  |
| PLL, OSC                                     | 16KB D-cache<br>w/ Parity Check  | 16KB I-cache<br>w/ Parity Check | 10/100 ENET w/ IEEE® 1588 |                   |                    | S/PDIF Tx/Rx             |  |
| Resource Domain Control                      | FPU MPU  | NVIC                            | 1Gbps ENET w/ AVB         |                   |                    | 6 x SPI                  |  |
|  | 256 KB TCM w/ ECC  |                                 | 1Gbps E                   | 1Gbps ENET w/ TSN |                    | 12 x UART                |  |
| Secure JTAG, SWD                             | Multimedia  2D GPU with Vector Graphics Acceleration   |                                 | 2 x                       | 2 x FlexIO        |                    | 2 x USB 2.0 OTG w/ PHY   |  |
| Semaphore                                    | 2D Graphics Acceleration (PXP)<br>Resize, CSC, Overlay, Rotation   |                                 | Timers                    |                   |                    |                          |  |
|  |  |                                 | 1 x EWM                   |                   | 4 x Quadrature ENC |                          |  |
| Temp Monitor                                 | MIPI® CSI  | Parallel CSI                    | 4 x FlexPWM               |                   | 4 x QuadTimer      |                          |  |
|  | MIPI DSI   | Parallel LCD                    |                           |                   |                    |                          |  |
| Internal Memory                              | External Men   | External Memory                 |                           | 6 x GP Timer      |                    | 4 x Watchdog             |  |
| Up to 2MB SRAM Total                         | Dual Channel QSPI FLASH x2 w/ Encrypted Execution<br>HyperRAM™/HyperFLASH™/PSRAM   |                                 |                           | A                 | alog               |                          |  |
| (Configurable ECC)                           |  |                                 |                           | DC 4.2 Msps       | 4 x Analog         | Comparator w/ 8b DAC     |  |
| ROM  | External Memory Controller w/ Memory Crypto Engine<br>8/16/32-bit SDRAM/LPSDRAM<br>8/16-bit Parallel NAND/NOR Flash/FPGA/SRAM/8080 |                                 | 1 x 12b DAC               |                   |                    |                          |  |
|  |  | Security                        |                           |                   |                    |                          |  |
| AES-128/256 Code Watchdog                    | Timer DES/3DES   | eFuse                           | Elliptic Curve Cryptog    | raphy HA          | NB                 | Memory Crypto Engine     |  |
| RSA4096 Secure RA                            | AM Secure RTC  | SHA-1/SHA-2                     | SRAM PUF/UD               | F Tamper [        | Detection          | TRNG                     |  |
| ilable on certain products within the family |  |                                 |                           |                   |                    |                          |  |

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Note: The information on this document is subject to change without notice.

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